Chapter I Introduction

1-1. What is the differences between
i) µP and µC?, ii) CPU and µP iii) RAM and ROM
iv) ROM and PROM v) EPROM and EEPROM
vi) Buffer and Batch vii) Register and Memory location
1-2. What is the devices that can be supported by µC? give examples
1-3. State some devices used for input data, and others used for output data.
1-4. What is the function of data bus and Address bus, and what is the effect of size (bandwidth) of each on the computer system?
1-5. Why Address bus is unidirectional and both data bus and control bus are bidirectional?
1-6. What is the system software, and what is the main software which necessary to deal with a computer?
1-7. What is the first microprocessor introduced by Intel company and when that was (year)?. State its specifications in terms of: speed (frequency), number of data and address buses lines, number of registers, registers bandwidth and maximum memory space it can support
1-8. What is the last 4 general purpose microprocessors introduced by Intel, the 1st generation of the last 1 introduced in which year?
1-9. What is moor's law referring to?

Chapter II Computer System Overview

2-1. What are the following and the function of each, use sketches to show.
IR, PC, MDR, MAR, MBR, ABR
2-2. by assuming that instruction (**sub a,b**) is stored at RAM location addressed by 1F09 show how this instruction will be transferred to CPU, use sketching to show. Why instruction should be transferred to CPU?
2-3. What are RISC and CISC referring to?
2-4. Compare between RISC and CISC in terms of:
I) complexity, state the main difference in hardware architecture which reflects the complexity (look to the block diagram of each).
II) number of instructions.
III) number of cycles per instruction.
IV) power consumption.
V) number of code lines to do same process(code density).
VI) efficiency.
VII) cost.
VIII) number of transistors.
2-5. Are your laptops or lab PCs(desktops) CISCs or RISCs?
2-6. What is the main function of coprocessor, and is it a general purpose processor or special processor?
2-7. What is the computer architecture?
2-8. What is ISA?. Explain that by sketching the layers ordered from basic hardware to highest level of software, show where is ISA location in the sketch. Referring to that sketch, what is the main function of ISA?
2-9. Break down a computer problem-, use sketch, starting by problem and ending by transistors
2-10. State the differences between high level , assembly, and machine languages in terms of:
I) representation form
II) ease of use and tracing
III) execution speed
IV) memory space required
V) level order(highest to lowest)
VI) machine dependence
2-11. What is the difference between Von Neumann and Harvard architectures models?, show by sketch
2-12. What is SHARC architecture referring to? is it applying for general purpose processor or special processor?
2-13. Are your laptops or lab desktops microprocessors are Von Neumann, Harvard or SHARC models?
2-14. What is the relation between bit, nibble, byte, word, double word, long word, quad word?
2-15. What is the main function of clock in a CPU?
2-16. What is ALU and what its function?
2-17. What is the function of CPU general purpose registers in general?

Chapter III - Intel 8086 Microprocessor

3-1. What DIP refers to? use sketch to show..
3-2. Compare between Intel 8085 and Intel 8086 processors in terms of:
I) number of data/address lines
II) number of flags
III) maximum memory space can be supported.
IV) min/max mode support.
V) memory segmentation support.
VI) pipelining support.

3-3. what is min/max mode means in Intel 8086?
3-4. Relating to data and memory Access, what is the meaning of data endianness?
3-5. Show how data can be stored using big and little endians, show by example and sketch.
3-6. Intel processors use which endianness?- big or little?

Intel 8086 architecture

3-7. What are the main units in Intel 8086 architecture? and what is the main function of each?
3-8. How many visible registers in Intel 8086 ?What are their bandwidths?
3-9. How many registers in BIU and what is the main function of each? briefly.
3-10. IP register is used to hold the effective address of next instruction of which memory segment?
3-11. In which 8086 unit, instruction queue is located, and what its size, its input source? and it's output destination?
3-12. How many registers in EU and what the main function of each? briefly
3-13. What are the EU registers that can be used as 2 registers of half size?
3-14. What is relation between registers AX and DX in execution of a 16 bits multiply instruction?
3-15. How many bits in flag registers, and how many bits of them are inactive(unused)?
3-16. briefly ,state the function of each flag bit
3-17. If we divide registers to groups related to their function. What are the general purpose registers, the pointer and index registers, the status registers and the segments registers?
3-18. Are BIU and EU work synchronously or asynchronously?
3-19. What is the maximum instruction length (bits or bytes) in 8086 ?
3-20. What is segmentation meaning in memory?
3-21. What is usual segments used in computer? and they should be of same size or what? They should be separated, overlapped or what?
3-22. Segmentation is usually done by CPU automatically or by programmer only or both?
3-23. Where the stack could be created and how its mechanism of data access?
3-24. What is the queue data access mechanism?
3-25. What the difference between segment starting address and offset, give example, use sketch if necessary?
3-26. What is the relation between effective address(EA), segment starting address and physical address(PA) ?
3-27. What is the relation between program counter (PC) and PA?
3-28. What is the relation between effective address and offset?
3-29. If CS register contents = 5A0C and IP register contents =1C3A, what the value of PA will be?
3-30. What is the purpose of PC (Program Counter), what it's bandwidth in 8086 and what its relation to Address bus lines?

Instruction Format and Pipelining

3-31. What is the instruction cycles?
3-32. What is the instruction format referring to?
3-33. What is the contents of an instruction in general?
3-34. What the minimum/maximum operands for an instruction?
3-35. What are source and destination meaning in an instruction?
3-36. What instructions pipelining means?, show by sketch if needed
3-37. What is throughput in instructions pipelining?
3-38. What is latency in instructions pipelining?
3-39. What is the advantages (pros) of instructions pipelining
3-40. What is the disadvantageous (cons) of instructions pipelining?
3-41. A CPU uses instructions pipelining for 6 instructions, each instruction consists of 5 stages **(1-fetch => 2-decode =>3-execute => 4-read data =>5-write result).** By assuming that each stage takes 1 clock cycle, 1 clock cycle = 5ns, latency = 0 and all instructions are completely independent, (a) what is the time needed to finish all the process of the 6 instructions?. (b) write an expression to calculate the time needed to finish all the process of n instructions of k stages.

Addressing Modes

3-42. What Addressing mode in a computer means?
3-43. What the difference between register and register indirect addressing modes?, you can show by sketch.
3-44. What is the difference between memory indirect and register indirect addressing modes?, you can show by sketch.
3-45. What is the downside (disadvantageous) and upside (advantageous) of indirect memory addressing mode.